CLAIMS:

1. Apparatus for transmitting an n-bit digital signal across an interconnect, where n is the width of said interconnect, the apparatus comprising means for converting said digital signal into its low swing equivalent, the apparatus being characterized by means for encoding said signal, prior to transmission thereof.

2. Apparatus according to claim 1, wherein the encoding is targeted for low energy characterized by reducing the number of bits which change in a current signal to be transmitted relative to the bits of the signal transmitted previously.

3. Apparatus according to claim 1, wherein the encoding is targeted for reducing crosstalk induced noise.

4. Apparatus according to claim 1, wherein the encoding is targeted for reducing crosstalk induced delay.

5. Apparatus according to claim 1, wherein the encoding is targeted for increasing robustness of the data transmitted.

6. Apparatus according to any one of the preceding claims being used in respect of programmable logic devices, specifically FPGAs (embedded or stand-alone), to reduce energy increase robustness by improving signal integrity, reducing crosstalk, and/or reduce delay.

7. Apparatus according to claim 1, wherein the means for encoding said signal comprises means for comparing the values of the current signal to be transmitted with the values of a signal transmitted previously, determining whether or not the number of bits of said current signal which are of opposite value to the corresponding bits of the previous signal exceeds some predetermined threshold value, and only encoding said current signal if said predetermined threshold value is exceeded.

8. Apparatus according to claim 7, wherein if the width of the interconnect being coded is even, the predetermined threshold value is n/x, where x is an even integer.

9. Apparatus according to claim 8, wherein $x = 2$.

10. Apparatus according to claim 7, wherein if the width of the interconnect being encoded is odd, the predetermined threshold value is $[(n + 1)/2] - 1$.

11. Apparatus according to any one of claims 1 to 10, further including a receiver.

12. Apparatus according to claim 11, wherein the type of encoding employed by said encoding means is bus invert coding, whereby if the number of bits that "flip" exceeds the predetermined threshold value, all of the bits of the current signal to be transmitted across the interconnect are inverted prior to transmission thereof, and an "invert" signal is also transmitted, to indicate to said receiver that said signal has been inverted.

13. A method for transmitting an n-bit digital signal across an interconnect, where n is the width of said interconnect, the method comprising the steps of converting said digital signal into its low swing equivalent, and being characterized by the step of encoding said signal, prior to transmission thereof.

14. A method according to claim 13, wherein said step of encoding said signal comprises the steps of comparing the values of the current signal to be transmitted with the values of a signal transmitted previously, determining whether or not the number of bits of said current signal which are of opposite value to the corresponding bits of the previous signal exceeds some predetermined threshold value, and only encoding said current signal if said predetermined threshold value is exceeded.

15. A method according to claim 14, wherein if the width of the interconnect being encoded is even, the predetermined threshold value is n/x, where x is an even integer.

16. A method according to claim 15, wherein $x = 2$.

17. A method according to claim 14, wherein if the width of the interconnect being encoded is odd, the predetermined threshold value is $(n + 1)/2 - 1$.

18. A method according to any one of claims 13 to 17, including the step of providing a receiver for receiving the transmitted signal.

19. A method according to claim 18, wherein the type of encoding employed is bus invert coding, whereby if the number of bits that "flip" exceeds the predetermined threshold value, all of the bits of the current signal to be transmitted across the interconnect are inverted prior to transmission thereof, and an "invert" signal is also transmitted, to indicate to the receiver that signal has been inverted.